

Amendment  
Serial No. 10/760,475  
Attorney Docket No. 001681A

### **REMARKS**

Claims 24-37 are pending in the present application and are rejected. Claims 24-28 and 31-37 are herein amended.

#### **Applicants' Response to Objections to the Specification**

The Office Action objects to the title of the invention, stating that it is not descriptive. In response, Applicants herein amend the title as follows:

**SEMICONDUCTOR INTEGRATED CIRCUIT RELATED TO A CIRCUIT  
OPERATING ON THE BASIS OF A CLOCK SIGNAL**

Applicants submit that the amended title is sufficiently descriptive. Favorable reconsideration is requested.

#### **Applicants' Response to Double Patenting Rejection**

The Office Action argues that although the claims are not identical, they are not patentably distinct from each other because each and every limitation in claims 24-28 and 31-35 of the instant application read on the claims of the U.S. Patent No. 6,707,328 (the '328 Patent).

Because both the cited reference and the present application are commonly assigned, Applicants herewith file a Terminal Disclaimer signed by the Attorney of Record, disclaiming any patent term of the present application that would extend beyond the patent term of the cited patent. A Power of Attorney and Correspondence Address Indication Form and a Statement

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under 37 C.F.R. §3.73(b), both signed by a party authorized to act on behalf of the assignee is submitted herewith. Applicants submit that the rejection has been overcome.

**Applicants' Response to Claim Rejections under 35 U.S.C. §112**

**Claims 24-37 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention.**

The Office Action states that claims 24 and 31 are indefinite because it is impossible to have an independent potential on the first power supply wire with respect to the second power supply wire. It is noted that the input terminal receives a single voltage from the external power supply and both power supply wires are coupled to the input terminal and source of electric potential.

In response, Applicants herein amend claims 24 and 31 in order to more clearly recite that the power supply wires are independently formed, rather than having an independent potential. Furthermore, Claim 25 was rejected because there the claim repeats the same limitation twice. Applicants herein amend the claim to correct this error.

Although the Office Action did not make such a rejection, we note that several of the claims as filed in the preliminary amendment contain improper dependencies. The Examiner had contacted Applicants' representative prior to issuing the Office Action requesting clarification. Applicants' representative informed the Examiner of the correct dependencies; however, there is

no mention in the Office Action of the conversation with the Examiner. Therefore, Applicants also amend the claims to recite the correct dependencies as given to the Examiner.

**Applicant's Response to Claim Rejections under 35 U.S.C. §102**

**Claims 24-37 were rejected under 35 U.S.C. §102(b) as being anticipated by Bonneau et al (U.S. Patent No. 4,988,893).**

It is the position of the Office Action that **Bonneau** discloses the invention as claimed. **Bonneau** discloses in Figure 2A a Polarity Hold Shift Register Latch having master and slave sections. Master section M2 contains inverters I22 and I23. Master section M2 is connected to inverter I21, which is connected to both positive voltage Vdd and ground Gnd.

The Office Action argues that master section M2 and slave section S2 are a plurality of logic circuits, that inverter I22 is a first circuit, and that inverters I22 and I23 are together a second circuit. The Office Action further argues that the line between transistor P21 and positive voltage Vdd is a first power supply line and the line between transistor P24 and positive voltage Vdd is a second power supply line. The Office Action notes that these two lines are independent from each other. It is unclear what is regarded as an input terminal, but it appears that the Examiner believes that positive voltages Vdd (connected to P21) and Vdd (connected to P24) are input terminals.

The application discloses a plurality of logic circuits, each having a first circuit 13 and second circuit 6. In the simplest embodiment of the invention, a first power supply wire 7 and a

second power supply wire 8 are both connected to a first input terminal 2, as illustrated in Figure 1. The other end of first power supply wire 7 is connected to first circuit 13, while the other end of second power supply wire 8 is connected to second circuit 6. As is evident from the Figures, the two power supply lines are independently formed from each other, and both are connected to the first input terminal 2.

In response, Applicants respectfully argue that **Bonneau** does not disclose a semiconductor device as recited by independent claim 24. The line of **Bonneau** which the Office Action regards as a “second power supply line” (the line between P24 and Vdd) is not connected to an input terminal. That line is only connected to a positive voltage Vdd of inverter I22, not to an input terminal which receives an externally supplied power supply voltage. These first and second power supply wires must be connected to the same input terminal, since claim 24 only recites a single input terminal. Thus, **Bonneau** does not disclose “a second power supply wire formed on said semiconductor substrate independently of said first power supply wire and connected between said input terminal and said second circuit of each of said plurality of said logic circuits.” For at least these reasons, Applicants respectfully traverse the rejection.

With regard to the dependent claims, Applicants respectfully argue that they are patentable due to their dependency on claim 24, which Applicants argue is patentable for the reasons stated above. With regard to claim 31 and claims dependent thereon, the Office Action states that these claims are rejected for the same reasons as the rejection of claim 24. Therefore, Applicants also traverse these claims on the same grounds as claim 24, as discussed above.


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For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned agent.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,  
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